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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

My re patent application of:
Berthold et al.

MMB Docket No. **1890-0274**

Application No.: **10/563,040**

Filed: **December 30, 2005**

For: **Master Latch Circuit with Signal
Level Displacement for a Dynamic
Flip Flop**

Examiner: **Daniel E. Rojas**

Group Art Unit: **4125**

I hereby certify that this correspondence is being deposited
with the United States Postal Service as first class mail in
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David R. Moorman

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April 15, 2008

Date of Signature

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, Applicants hereby disclose the following reference(s)
regarding the above-identified patent application.

Articles:

- 1) Partovi et al. "Flow-Through Latch and Edge-Triggered Flip-Flop Hybrid Elements." IEEE International Solid-State Circuits Conference. 1996. (2 pages).
- 2) Klass et al. "A New Family of Semidynamic and Dynamic Flip-Flops with Embedded Logic for High-Performance Processors." IEEE Journal of Solid-State Circuits. Vol. 34, No. 5. May 1999. 712-716. (5 pages).

04/17/2008 HAL133 00000001 10563040

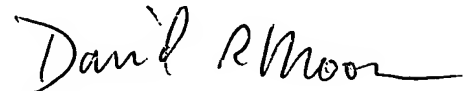
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Pursuant to 37 C.F.R. § 1.17(p), enclosed please find a check in the amount of \$180.00 for the Information Disclosure Statement filing fee. The Commissioner is hereby authorized to charge any deficiency or to credit any overpayment to Deposit Account No. 13-0014, but not to include any payment of issue fees.

April 15, 2008
Maginot, Moore & Beck
Chase Tower
111 Monument Circle, Suite 3250
Indianapolis, Indiana 46204-5109
(317) 638-2922 phone
(317) 638-2139 fax

Respectfully Submitted,


David R. Moorman
Attorney for Applicants
Registration No. 59,323